UNITED STATES PATENT APPLICATION

FOR

ENABLING CIRCUIT FOR AVOIDING NEGATIVE VOLTAGE TRANSIENTS

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CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation-in-part application of US Nonprovisional Application Ser. No. 10/176,141 filed June 20, 2002, all the teachings of which are incorporated herein by reference.

FIELD OF THE INVENTION

This invention relates to an enabling circuit for avoiding negative voltage transients from an associated regulating circuit, and more particularly to such an enabling circuit for enabling a synchronous rectifier converter to switch from a first state to second state if the charge on an energy storage element of the synchronous rectifier converter is less than a reference charge.

BACKGROUND OF THE INVENTION

A variety of circuits have energy storage element such as capacitors, inductors, and transformers that transfer energy from an input to an output of such circuits. If such energy storage elements are not properly discharged in some instances, unwanted power disturbances, e.g., negative voltage transients, may occur in the output signal causing damage to nearby sensitive components.

For instance, such a regulating circuit may be a DC-DC converter. DC-DC converters generally accept a DC input at one voltage level and convert it to a DC output at a higher or lower voltage level. Such DC-DC converters may be used in a wide variety of electronic devices in conjunction with a variety of systems. One such system may be used to provide a battery

charging function for portable electronic devices such as laptop computers, cell phones, pagers, personal digital assistants, and the like.

One type of DC-DC converter is a synchronous rectifier converter (SRC). An SRC does not use any Schottky diodes, but rather uses transistors referred to as "synchronous rectifiers." Such transistors may be a variety of transistors such as MOS or MOSFET transistors. An SRC may also have a variety of internal components that typically include an energy storage element, e.g., a capacitor, inductor, or transformer, with one or more transistors controlled by various control techniques, e.g., pulse width modulation where the switch frequency is constant and the duty cycle varies with the load.

When an SRC is used in conjunction with a battery power management system, the SRC may accept an input voltage from a number of different power sources and convert it to an appropriate output voltage to, among other things, provide an appropriate charging current to an associated rechargeable battery. In such a battery power management system, there is typically an associated controller used to control the battery charging process. Such controller may be an integrated circuit (IC) having a plurality of input terminals or pins, some of which are connected to the output of the SRC. For instance, two such terminals may be coupled to either side of a sense resistor. The sense resistor may be in series with the output of the SRC such that it provides a signal representative of the charging current provided at the output of the SRC.

If a soft start occurs when the energy storage element, e.g., a capacitor, of the SRC is charged at a significant value, e.g., over several volts, negative voltage transients may appear on either terminal of the sense resistor potentially causing catastrophic failure of the associated controller IC. Accordingly, there is a need for an enabling circuit and method that overcomes the above deficiencies in the prior art and is capable of avoiding negative voltage transients from an

associated regulating circuit by enabling the regulating circuit only when the charge on the energy storage element is below a reference charge.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention, together with other objects, features and advantages, reference should be made to the following detailed description which should be read in conjunction with the following figures wherein like numerals represent like parts:

FIG. 1 is a block diagram of a system including an enabling circuit consistent with the present invention for enabling an associated regulating circuit to switch from a first state to a second state;

FIG. 2 is a block diagram of an exemplary enabling circuit consistent with the invention for enabling an associated synchronous rectifier converter to switch from one state to another state;

FIG. 2A is a circuit diagram illustrating an exemplary embodiment of the enabling circuit of FIG. 2;

FIG. 3 is a block diagram of a battery management system utilizing the enabling circuit of FIG. 2; and

FIG. 4 is a block diagram of another embodiment of an exemplary enabling circuit in a battery charging system.

DETAILED DESCRIPTION

Turning to FIG. 1, an exemplary system 100 including an enabling circuit 104 and an associated regulating circuit 102 is illustrated. The regulating circuit 102 may be any variety of

circuits, e.g., a synchronous rectifier converter, containing an energy storage element 106, e.g., a capacitor. In general, the enabling circuit 104 monitors the charge on the energy storage element 106 and enables the regulating circuit 102 to switch from a first state to a second state when the charge on the energy storage element is below a reference charge. The first state may be any variety of states such as a power off state, and the second state may also be any variety of states such as an operating state where the regulating circuit 102 is controlled by a particular control technique. The reference charge should be chosen based on the particular system and sensitivity of associated components. In one embodiment, the reference charge may be 3.0 volts.

The enabling circuit 104 has one input terminal 107 configured to accept a signal, Vdsch, representative of an acceptable reference charge level for the energy storage element 106. The enabling circuit 104 may have another input terminal 109 configured to accept a logic control signal chginh. Such logic control signal, chginh, has a predetermined state, e.g., low state, when at least one non energy storage element condition related to operation of the regulating circuit 102 is satisfied. Such a condition or conditions may be any variety of other conditions known to those skilled in the art unrelated to the charge on the energy storage element 106. For instance, one condition may be the proper coupling of an input power source at a proper power level to the input of the regulating circuit 102.

The enabling circuit 104 accepts a feedback signal from the regulating circuit 102 along path 119. Such feedback signal is representative of the charge on the energy storage element 106. The enabling circuit compares the charge on energy storage element 106 with a reference charge and may output an enabling signal if the charge level is less than the reference charge level. The enabling circuit 104 may also include various discharging means as further described

in reference to FIG. 2 in order to discharge the energy storage element 106 below the reference charge level should the charge be greater than the reference charge level.

In one embodiment, once the charge on the energy storage element 106 is below the reference charge, the enabling circuit 104 sends an enabling signal along path 115 to the controller 120. The controller 120 is responsive to the enabling signal to then enable the regulating circuit to switch from a first state, e.g., a non-operating state or a predetermined suitable operating state, to a second state, e.g., another operating state. As such, an enabling circuit 104 consistent with the invention may advantageously delay operation of the regulating circuit 102 in the second state while maintaining operation of the regulating circuit 102 in the first state until the energy storage element 106 is discharged below a reference charge.

In another embodiment, the enabling circuit 104 may not send an enabling signal to the controller 120 until both the energy storage element 106 is discharged below the reference charge level and a logic control signal, e.g., signal chginh, input to the enabling circuit is at a predetermined state. Such predetermined state is representative of at least one satisfactory non energy storage element condition. Such predetermined state may also be representative of a satisfactory condition for all other non energy storage element conditions. In this case, an enabling circuit 104 consistent with the invention delays switching the regulating circuit 102 to operation in the second state while maintaining operation of the regulating circuit 102 in the first state, e.g., a non-operating state or a predetermined suitable operating state, until the energy storage element 106 is discharged below a predetermined charge level and a signal representing at least one satisfactory non energy storage element condition related to operation of the regulating circuit is satisfied.

Turning to FIG. 2, one exemplary system 200 having an enabling circuit 204 consistent with the invention and a synchronous rectifier converter (SRC) 202 is illustrated. The SRC accepts an input voltage signal at input terminal 226 and provides an output voltage signal at output terminal 211. The SRC may include an inductor 208, a capacitor 206 and switches K1, K2. Switches K1, K2 may be any type of transistors and for simplicity are drawn to represent MOS type transistors. Such switches K1, K2 may be controlled by a variety of control techniques such as pulse width modulation (PWM) where the switch frequency is constant and the duty cycle varies with load, pulse-frequency modulation, or current-limited pulse-frequency modulation as those control techniques are known to those skilled in the art.

The enabling circuit 204 may include a comparator circuit 232, an output decision circuit 234, and discharge path including resistors R1, R2 and switches K3, K4. The comparator circuit 232 may be any variety of circuits for comparing the charge on the capacitor 206 to a predetermined reference value charge represented by control signal Vdsch input to the comparator circuit. The comparator circuit 232 is configured to provide an output signal to maintain the SRC 202 in the first state, e.g., a non-operating state or a predetermined suitable operating state, if the charge on the capacitor 206 is higher than the reference charge. The comparator circuit 232 is also configured to provide output signal to switch the SRC 202 from the first state to a second state, e.g., another operating state where switches K1, K2 are under control of the controller 220, if the charge on the capacitor 206 is less than the reference charge.

The output decision circuit 234 may be any variety of circuits for performing a desired logic function. The output decision circuit 234 accepts the output signal dsch from the comparator circuit 232 and may further accept a logic signal chginh from a separate source. The output decision circuit 234 may be configured to output an enabling signal on path 215 to the

controller 220 if signal dsch indicates the charge on the capacitor 206 is less than a reference charge level. The output decision circuit 234 may alternately require signal dsch to indicate the charge on the capacitor 206 is less than a reference charge level, and require signal chginh to be in a predetermined state, e.g., low state, when at least one non energy storage element condition is satisfied. The output decision circuit 234 is not a necessary part of the enabling circuit 204 if the logic signal chginh is not input to the enabling circuit. In this case, the comparator circuit 232 would provide the enabling signal if the charge on the capacitor 206 is less than the reference charge.

The enabling circuit 204 may also include a discharge path including resistors R1, R2, and switches K3, K4 to discharge the capacitor 206 below a reference level. Switches K3, K4 may be any type of transistors and for simplicity are drawn to represent MOS type transistors. Detailed operation of an enabling circuit and the discharge path is made later with reference to the exemplary enabling circuit of FIG. 2A.

Turning to FIG. 2A, a circuit diagram of one exemplary enabling circuit 204a is illustrated. Those skilled in the art will recognize a variety of circuit configurations which may be utilized in an enabling circuit consistent with the present invention. In the exemplary embodiment of FIG. 2A, the comparator circuit 232 of FIG. 2 includes a comparator 232a having its positive input terminal accepting the input signal representative of the charge on the capacitor 206 and its negative input terminal accepting the other input control signal, Vdsch, representative of a reference value charge.

The output decision circuit 234 includes a NOR gate 234a. The NOR gate 234a accepts the output from the comparator 232a and the control signal chginh. The output of the NOR gate 234a is HIGH only if all inputs are LOW. Otherwise, the output of the NOR gate 234a is LOW.

In this embodiment, the enabling signal sent by the enabling circuit 204 to the controller 220 to enable the regulating circuit 202 to switch from the first state, e.g. switches K1, K2 open, to the second state state, e.g., switches K1, K2 under control of controller 220, is sent when the output of the NOR gate is HIGH.

Operation of the exemplary enabling circuit 204a in conjunction with the system 200 is described further herein with reference to the Truth Table of Table 1. Table 1 details the status of the various control signals and switches relative to each other with the output decision circuit 234 functioning as the NOR gate 234a of FIG. 2A. The status of control signal chginh input to the enabling circuit 204, control signal dsch output from comparator 232a, control signal chgen output from the NOR gate 234a, switches K1, K2 of the SRC 202, and switches K3, K4 of the enabling circuit 202 are all detailed in Table 1.

TABLE 1

chginh	H	H	L	L
dsch	H	L	H	L
chgen	L	L	L	H
K1	OFF	OFF	OFF	PWM
K2	OFF	OFF	OFF	PWM
K3	ON	ON	ON	OFF
K4	ON	ON	ON	OFF

As illustrated and described more fully herein, the exemplary enabling circuit 204a advantageously does not enable switches K1, K2 of the SRC 204 to be controlled by the proper control technique, e.g., PWM control, and maintains switches K1, K2 in an OFF position, until the capacitor 206 of the SRC 204 is discharged below a reference charge (control signal dsch is L), and at least one other non capacitor charge related condition for operation of the regulating

circuit (control signal chginh is L) is satisfied. As such, negative voltage transients that may otherwise occur at the output terminal 211 of the SRC 204 are avoided.

As illustrated in the first substantive column of Table 1, if the charge level on capacitor 206 is greater than a reference charge level as represented by control signal vdsch input to the comparator 232a, then the control signal dsch output from the comparator 232a is HIGH. The output control signal dsch from the comparator 232a is then input to the NOR gate 234a.

The other input to the NOR gate 234a may be the control signal chginh from a separate source. Such control signal chginh is representative of at least one non capacitor related condition pertinent to operation of the SRC 202. In this embodiment, if this chginh signal is LOW, at least one and perhaps all other non capacitor related conditions pertinent to operation of the SRC 202 are satisfactory. If this chginh signal is HIGH, such condition or conditions are unsatisfactory. Accordingly, if the output control signal dsch from the comparator 232a is HIGH and the chginh signal is also HIGH, the output signal from the NOR gate 344a is LOW. Thus, switches K1 and K2 remain OFF or open and the operation of the SRC 202 is delayed. As such, if the SRC is operating to provide a charging current to an associated rechargeable battery, such charging current would not be provided in this instance, nor would current flow from the capacitor 206 through the inductor 208 be possible in this instance.

Turning to the second substantive column of Table 1, if the capacitor 206 is discharged below the reference charge represented by control signal vdsch, the output control signal dsch from the comparator 232a goes LOW indicating the charge level on the capacitor 206 is acceptable. However, if another non capacitor charge related condition is unsatisfactory, the control signal chginh remains HIGH. As such, the output of the NOR gate 234a remains LOW and the operation of the SRC 202 is still delayed.

Turning to the third substantive column of Table 1, if the control signal chginh is LOW representing a satisfactory starting condition for at least one non-charge related condition, but the output control signal dsch from the comparator 232a is HIGH, then the output signal chgen from the NOR gate 234a remains LOW. As such, the operation of the SRC 202 is still delayed.

As illustrated in the fourth substantive column of Table 1, it is not until the capacitor 206 is discharged below the reference charge level (control signal dsch output from the comparator 232a is LOW), and at least one if not all other non-charge related conditions for operation of the regulating circuit (control signal chginh is LOW) are satisfied, that the control signal chgen output of the NOR gate 234a is HIGH. Once the control signal chgen is HIGH, switches K3 and K4 of the enabling circuit 202 open or are in an OFF position. The HIGH control signal chgen enables the controller 220 to drive the SRC 202. Hence, switches K1, K2 are controlled by an appropriate control technique, e.g., PWM.

If the enabling signal is not present in this embodiment, switches K3, K4 are closed or in an ON position. A discharge path for the capacitor 206 is then created through the switches K3, K4. Switch K3 is further coupled in series to resistor R1, while switch K4 is further coupled in series to resistor R2. Resistor R1 has a resistive value that is higher than the resistive value for resistor R2. As such, when switches K3, K4 are closed because no enabling signal from the NOR gate 234a is present, a discharge path is created and resistor R2 serves to discharge the capacitor 206.

Turning to FIG. 3, an exemplary battery charging system 300 generally including a power source 344, an SRC 302, an enabling circuit 304 consistent with the invention, a rechargeable battery 340, and a battery charging controller 320 is illustrated. Such a battery charging system 300 may be used in a variety of portable electronic devices such as laptop

computers, cell phones, pagers, personal digital assistants, and the like to provide and control power flow to a rechargeable battery 340, e.g., a lithium, nickel-cadmium, or nickel-metal hydride battery.

A sensor such as sense resistor 346 may be used in order to provide a sensed signal to the controller 320 indicative of the charging current Ichg to the battery. Such a controller 320 is typically an integrated circuit (IC) and may be sensitive to negative voltage transients that may otherwise occur at either terminal 349, 351 if the energy storage element 306 is not properly discharged below a reference charge value. Such negative voltage transients may appear on either terminal 349, 351 due to oscillation induced by an inductor and capacitor group of the SRC 302.

Once a power source 344 is properly coupled to the system 300, it provides an input DC voltage signal to the SRC 302. The power source 344 may be an AC/DC adapter configured to receive conventional AC voltage from a power outlet and convert it to an applicable DC voltage, or a DC/DC adapter such as a "cigarette lighter" type adapter configured to plug into that type of socket, or other types of power sources.

Advantageously, the SRC 302 accepts power input from the power source 344 and converts it to a proper output voltage and current level for providing a charging current Ichg to the battery 340 only if the controller 320 receives an enabling signal from the enabling circuit 304 along path 315. Otherwise, the controller 320 delays providing a charging current Ichg to the battery 340, while keeping the SRC 302 in a predetermined suitable state. This predetermined suitable state may be any variety of states as determined by the position of various switches in the SRC 302. In the previous embodiment of FIG. 2, switches K1, K2 of SRC 202

were chosen to be in an open state. The SRC 302 is controlled by the controller 320 by any variety of control techniques, e.g., PWM, known by those skilled in the art.

Advantageously therefore, the enabling circuit 304 delays providing of the charging current Ichg to the battery 340 until the energy storage element 306 is discharged below a reference charge. The enabling circuit 304 may also further delay the charging current Ichg to the battery 340 until another control signal, e.g., signal chginh, from another source indicates that at least one non-charge related condition pertinent to operation of the SRC 302 is satisfactory.

In another embodiment, FIG. 4 illustrates a battery charging system 400 generally including a DC power source 444 for providing power to recharge the rechargeable battery 440. Battery charging conditions may be controlled by the charging circuit 411 which regulates the output of the DC to DC converter 402. The charging circuit 411 may include an enabling circuit 404 consistent with another embodiment as further detailed herein.

The DC to DC converter 402 may be any variety of DC to DC converters controlled by any variety of control signals. The DC to DC converter 402 may be a synchronous rectifier converter having a high side switch K1, a low side switch K2, an inductor 408, and a capacitor 406 as is known in the art. A control signal from the charging circuit 411 may be output the low side terminal 415 and high side terminal 417 to the respective control terminals of the low side switch K1 and high side switch K2. In one instance, the switches K1, K2 may be any variety of transistors such as MOS transistors. The control signal may be a PWM signal where its duty cycle controls the duration of a "switch ON" state (high side switch K1 ON and low side switch K2 OFF) and "switch OFF" state (high side switch K1 OFF and low side switch K2 ON) and hence the output voltage and current level of the DC to DC converter 402.

If the charge on the capacitor 406 of the DC to DC converter 402 is above a reference value, the battery 440 is not electrically coupled to the output of the DC to DC converter 402 (switches K3 and K4 are OFF) and the charging circuit 411 instructs the DC to DC converter 402 to switch to a switch OFF state, and the capacitor 406 may discharge current via the inductor 408 and the closed switch K2 to ground. This may then cause undesirable power conditions on the terminals 418 and 419 of the charging circuit 411 that couple to either side of the sense resistor 449. For example, negative voltage transients and a negative current oscillation may be experienced at terminal 418 due to the parallel LC circuit (including inductor 408 and capacitor 406).

The charging circuit 411 may include another embodiment of an enabling circuit 404 that, like the other enabling circuit embodiments, prevents such undesirable power conditions on terminals 418, 419 in such instances. In general, during a soft start condition the enabling circuit 404 compares a charge on the capacitor 406 with a reference charge and does not enable the charging circuit 411 to control operation of the DC to DC converter 402 until the charge on the capacitor 406 is less than a reference charge. Therefore, the high side switch K1 and low side switch K2 of the DC to DC converter may remain OFF until an enabling signal from the enabling circuit 404 is received by the controller 490.

The enabling circuit 404 generally includes a comparison circuit 432, a switching circuit 434, a discharge path 436, and an output decision circuit 438. The comparator circuit 432 may include comparator 433. The comparator 433 may receive a first signal at its noninverting input terminal representative of a charge on the capacitor 406. The comparator may also receive a second signal at its inverting input terminal representative of a reference charge, represented by

signal Vdsch. The comparator compares such signals and provides an output comparison signal to the switching circuit 434 in response to the comparison.

The switching circuit 434 may accept the output comparison signal from the comparison circuit 432 and a soft start signal, e.g., as may be provided by the host power management unit (PMU) 480. The switching circuit 434 may then provide a first output signal to the output decision circuit 438 along path 483 and a second output signal to switch K5 of the discharge path 436. The switch K5 may be any variety of transistors such a MOS transistor. The switching circuit 434 may include an RS flip flop 435. The set terminal of the flip flop 435 may accept the soft start signal while the reset terminal may accept the comparison output signal. The output QB terminal of the flip flop 435 may provide the first output signal to the output decision circuit 438 while the other output terminal Q may provide the second output signal to the switch K5 of the discharge path 436.

The output decision circuit 438 may include any variety circuits for performing a desired logic function. In one embodiment, the output decision circuit may include an AND gate G1. The output decision circuit 438 provides a charge enable signal, chgen, to the controller 490 of the charging circuit 411. If the charge enable signal is digital one, then the controller 490 is able to control the pair of switches K1, K2 of the DC to DC converter 402, e.g., via a PWM control signal. If the charge enable signal is a digital zero, the controller 490 inhibits control of the pair of switches K1, K2 and the pair of switches may remain OFF. The controller 490 may include any variety of components to provide the control signal, e.g., a PWM signal, to the switches. For example, the controller 490 may include a plurality of error amplifiers to compare input signals of monitored parameters (not shown) with associated maximum thresholds for each parameter. The plurality of error amplifiers may then be configured as an analog "wired-OR" topology such

that the error amplifier that first detects a condition exceeding the associated maximum threshold controls the duty cycle of the PWM control signal.

In operation, the DC to DC converter 402 may initially be disabled having both switches K1 and K2 in an OFF state. In addition, both switches K3 and K4 may be OFF. Meanwhile, a digital one soft start signal may be received at the Set terminal of the flip flop 435 as requested by the PMU 480. The output Q of the flip flop 435 would then set to a digital one and the other output QB would be a digital zero. In response, the switch K5 of the discharge path 436 would close causing any charge on the capacitor 406 to be discharged via the path to ground created by the closed switch K5. In addition, since the QB output is a digital zero, the output of the AND gate G1 would also be a digital zero regardless of the CHG ON HOST signal from the PMU 480. The controller 490 may then be responsive to the digital zero signal from the AND gate G1 to inhibit control of the switches K1 and K2 and hence maintain the switches K1 and K2 in an OFF state.

The charge on the capacitor 406 continues to be discharged until it is discharged to a safe level below the reference charge level. Once the charge on the capacitor is less than the reference charge level, the output Q of the flip flop 434 would be a digital zero and the output QB of the flip flop 434 would be a digital one. Hence, the switch K5 of the discharge path would open. If the CHG ON HOST signal from the PMU 480 was also a digital one, then the output of the AND gate G1 (the enabling signal) would also be a digital one. In response, the controller 490 would then be able to control the state of the switches K1 and K2, e.g., via a PWM control signal. Advantageously, therefore if the controller 490 provided a PWM signal to place the switches K1 and K2 in a switch OFF state in such an instance, no adverse power

conditions would be created at terminals 418, 419 since the charge on the capacitor 406 has been sufficiently reduced.

There is thus provided an enabling circuit for enabling a DC to DC converter having a capacitor coupled to an output terminal of the DC to DC converter to be controlled by a control signal. The enabling circuit may comprise a comparison circuit configured to compare a first comparison signal representative of a charge on the capacitor with a second comparison signal representative of a reference charge and provide a comparison output signal in response to the comparison. The enabling circuit may also comprise a switching circuit configured to accept the comparison output signal, and in response to at least the comparison output signal provide a first switching signal in a first state if the charge on the capacitor is less than the reference charge; and an output decision circuit configured to accept at least the first switching signal and provide an enabling signal to enable the DC to DC converter to be controlled by the control signal in response to the first switching signal in the first state.

There is also provided a battery charging system comprising a DC to DC converter configured to accept an input power level from a DC power source and provide a regulated output power level to a rechargeable battery. The DC to DC converter may have a capacitor coupled to an output terminal of the DC to DC converter. The battery charging system may also include an enabling circuit for enabling the DC to DC converter to be controlled by a control signal. The enabling circuit may comprise a comparison circuit configured to compare a first comparison signal representative of a charge on the capacitor with a second comparison signal representative of a reference charge and provide a comparison output signal in response to the comparison. The enabling circuit may also comprise a switching circuit configured to accept the comparison output signal, and in response to at least the comparison output signal provide a first

switching signal in a first state if the charge on the capacitor is less than the reference charge; and an output decision circuit configured to accept at least the first switching signal and provide an enabling signal to enable the DC to DC converter to be controlled by the control signal in response to the first switching signal in the first state.

The embodiments that have been described herein, however, are but some of the several which utilize this invention and are set forth here by way of illustration but not of limitation. It is obvious that many other embodiments, which will be readily apparent to those skilled in the art, may be made without departing materially from the spirit and scope of the invention.